ABSTRACT

A design method of a logic circuit, capable of shortening the design period, is achieved by this invention. A semiconductor integrated circuit has a plurality of logic blocks each of which is constituted by a first logic circuit and a second logic circuit. Such semiconductor integrated circuit is designed in at least two steps: a first design step in which designing layout and timing verification are performed for a logic circuit including signal lines between the logic blocks and the first logic circuit; and a second design step in which layout and timing verification are performed for the second logic circuit in each logic block independently.